

FIG.1
RELATED ART

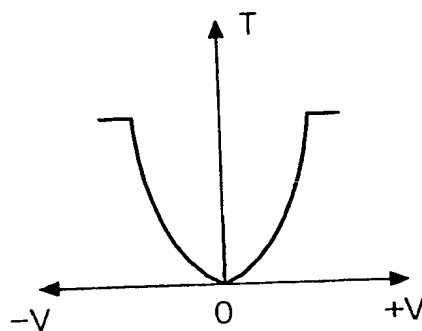


FIG.2
RELATED ART

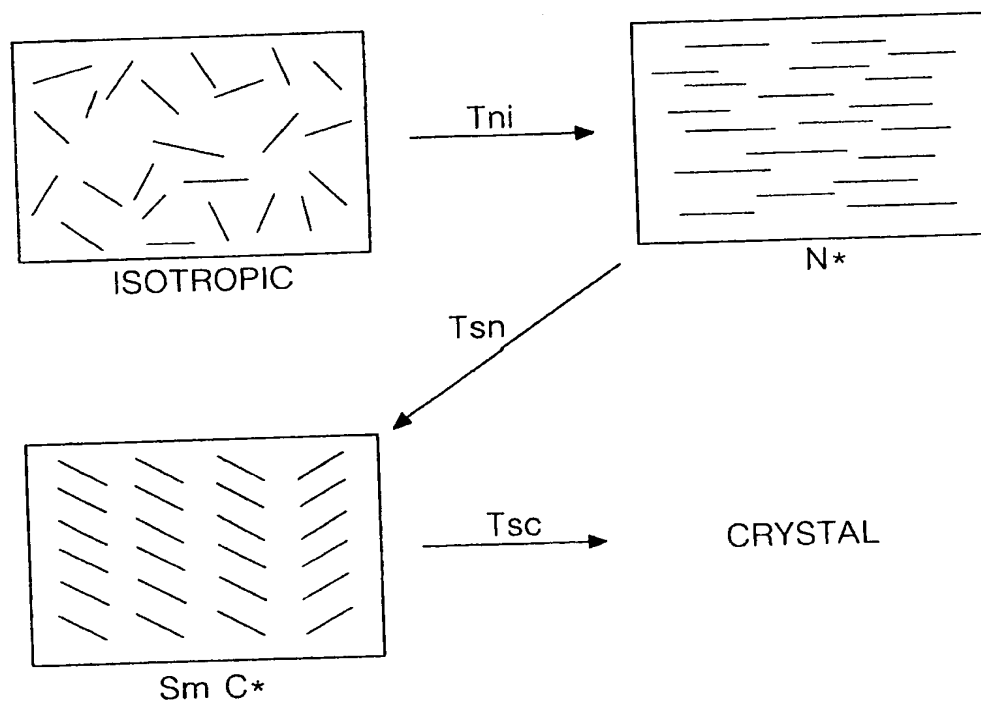
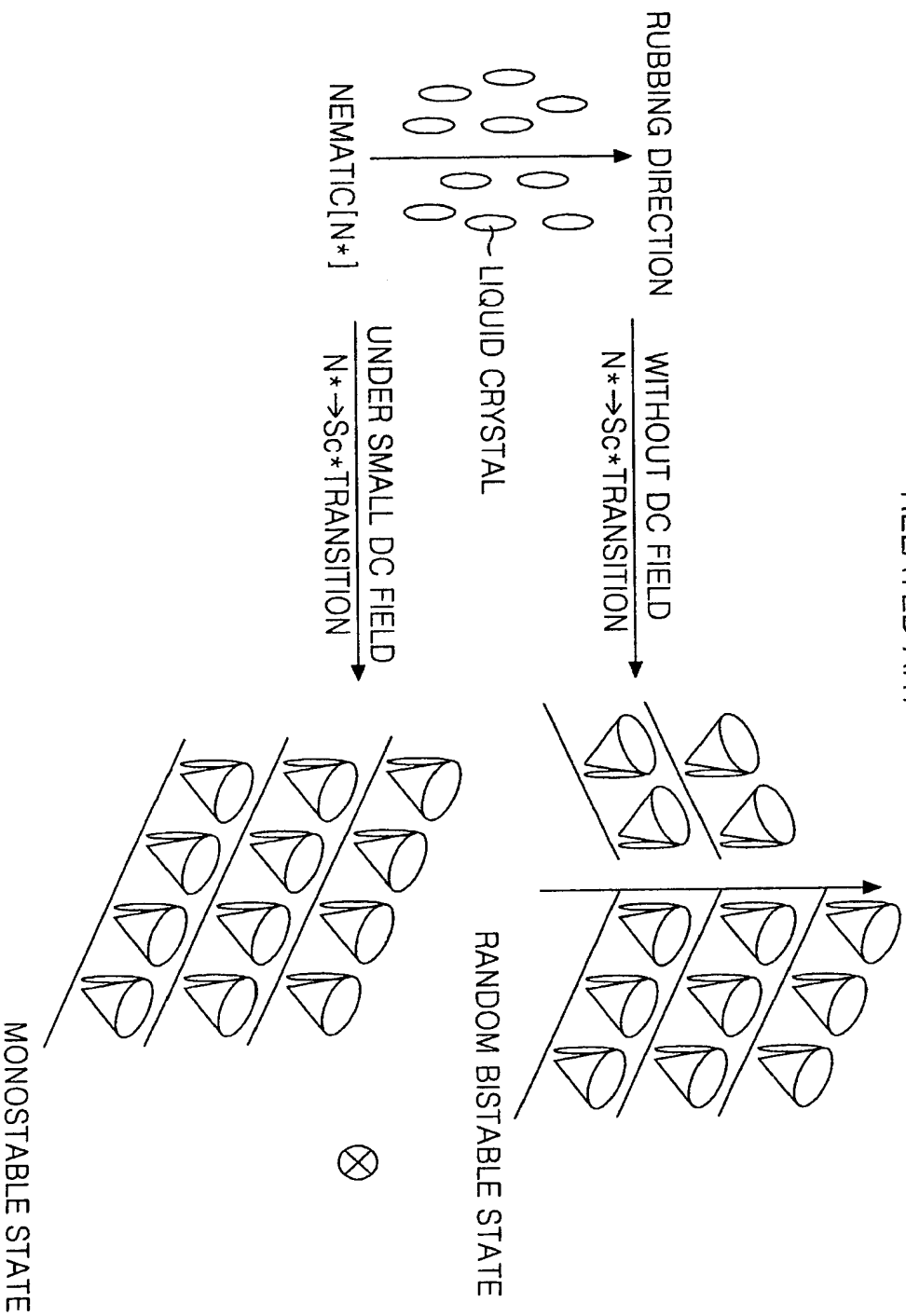


FIG. 3
 RELATED ART



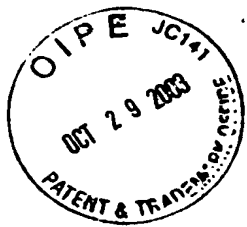


FIG.4A
RELATED ART

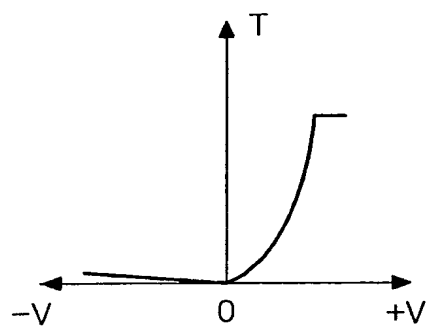


FIG.4B
RELATED ART

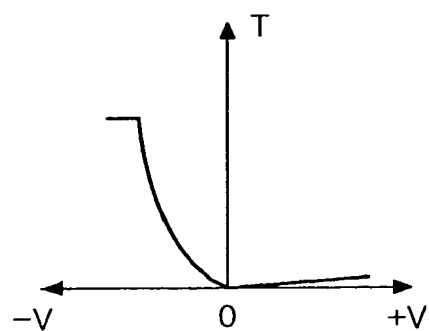




FIG.5A
RELATED ART

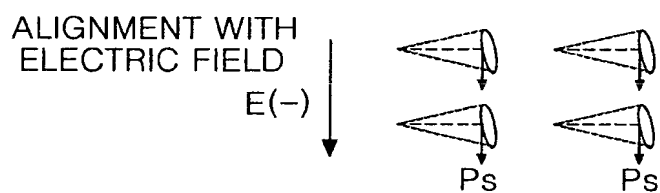
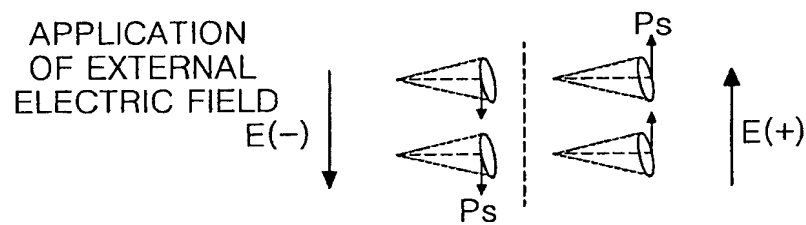


FIG.5B
RELATED ART



The diagram illustrates a pixel circuit architecture. At the top, input signals VH , VL , and V_{cc} are shown. A switch controlled by VH connects V_{cc} to a node connected to a capacitor (60) and a transistor (61). Another switch controlled by VL connects the same node to a common voltage source V_{com} . The other terminal of transistor 61 is connected to a horizontal bus line (72). This bus line passes through a series of transistors (64) which are also connected to vertical bus lines (68). On the left, a vertical stack of three rectangular components (66, 67, 68) represents the pixel's physical structure. The circuit includes multiple columns of pixels, labeled $DL1$, $DL2$, ..., $DLm-1$, DLm . Each column has its own set of gate lines ($GL1$, $IGL2$, ..., $GLn-1$, GLn) and data lines. Transistors (TFT) are used to connect the data lines to the pixel elements. Various nodes and connections are labeled with reference numerals such as 65a, 65b, 68a, 68b, 69, 71, 73, and 74.



FIG.7

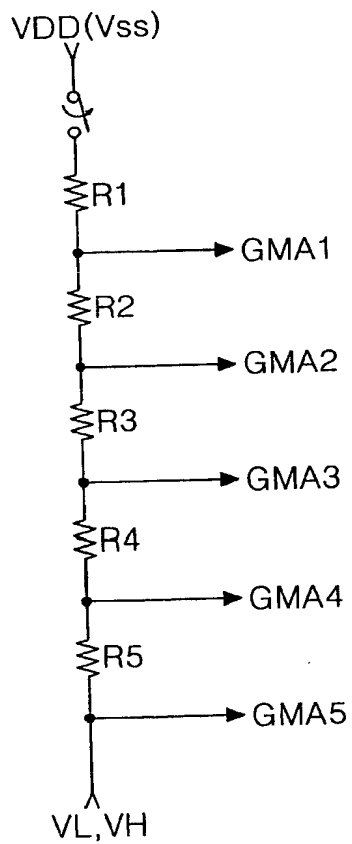


FIG.8

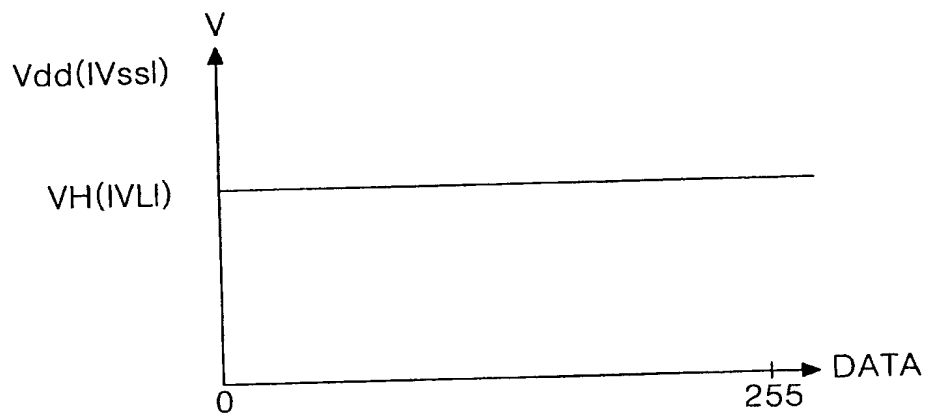




FIG.9

